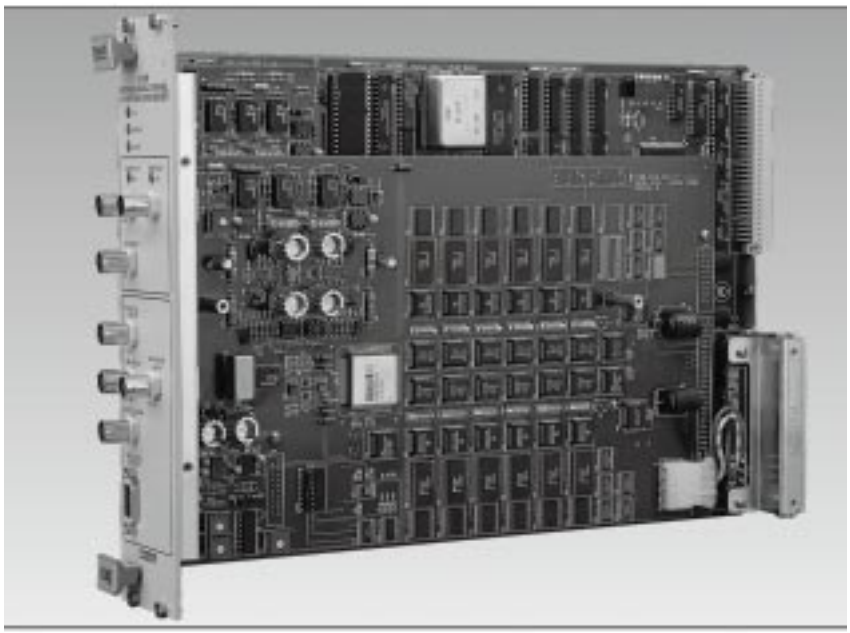
PRODUCT INFORMATION

500MS/s Dual Channel Waveform Synthesizer
Model 3162B



- **Arbitrary Waveform Generator 500MS/s Rate with 12-bit Resolution**
- **Phase Locking to Internal 1ppm Reference or to External Signals**
- **AM, PM and FSK Modulation Inputs and Real-time Frequency Hopping**
- **Waveform Sequences with Variable Clock Rates to Save Memory**
- **20ps Feature Placement and Jitter Resolution for Margin Testing**
- **CDMA Simulation and I&Q Modulation**

The 3162B Dual Channel Frequency Agile Waveform Synthesizer combines industry-lleading 500MS/s performance, frequency agility and modulation capability in a dual-slot VXIbus module. Signal output in the range of 100µHz to 200MHz with 12-bit resolution supports the test stimulus needs of the information age such as jitter injection with 20ps resolution, and I&Q modulation.

500Megasample/Second Performance
As products develop which use increased signal bandwidths, test equipment and systems are needed to keep pace with these trends. The 3162B's 500MS/s sample rate insures the production of test stimuli with the quality and performance necessary, e.g. harmonics are -40dBc for a 10MHz sine wave.

Frequency Agility
Racal met the demand for real-time frequency agility by providing the 3162B with an iinterface allowing the user to control the output frequency instantaneously. Up to 256 frequency hops are available at clock rates that are integer division ratios of the 3162B's sample clock. Hops are controllable via the front panel D-sub connector or triggered via the front panel or VXIbus.

Modulation Capability
External modulation capability is provided through the front panel inputs for Amplitude and Phase Modulation (AM and PM), as well as Frequency Shift Keying (FSK).

Phase Lock to External Signals
The 3162B automatically locks its output to external analog signals up to 18.75MHz. Phase offset resolution is programmable in 0.01° steps. The frequency of the external signal may be queried since the 3162B has a built-in 6-digit frequency counter.

Margin Testing

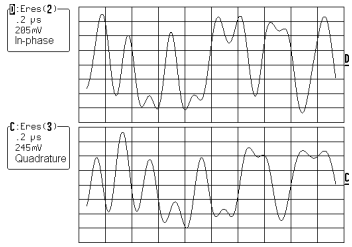
The 3162B can be used to analyze the sensitivity of a Unit Under Test (UUT) to variations in the time placement of features, i.e., edges, glitches, ripple, etc. The 3162B simulates these variations using either Feature Placement or Jitter Injection. These features are useful for simulating anomalies in disk drive read head signals or in digital communications data streams.

I&Q Simulation

The Model 3162B's two channel design with channel-channel jitter makes it ideal for simulating In-Phase and Quadrature (I&Q) modulation signals. I&Q waveforms can be created for the 3162B using math software like SystemView™ by Elanix or MatLab by MathWorks. The 3162B saves the communications system designer time in the design phase by simulating hardware, like encoders, filters and samplers using math software. The 3162B also speeds test system design by generating the most updated modulation schemes as an off-the-shelf product, saving the designer from having to develop dedicated test signal hardware. I&Q waveforms generated by the 3162B can then be connected to the I&Q inputs of a signal generator to produce the final RF test signal.

CDMA Link Example

The Code Division Multiple Access (CDMA) concept is designed to take sampled speech data, encode it, interleave it and use the Walsh coding scheme to spread data packets from many channels across a selected frequency spectrum. The codes are then scrambled, converted into I&Q, and filtered. Powerful math software can be employed to simulate the process of creating CDMA signals. The example given below is a model of an IS-95-A "Forward Link" traffic on channel 55. The data transmitted is a random binary sequence. This example was created using the optional CDMA library for the SystemView™ simulation tool from Elanix.



3162B Specifications

AMPLITUDE CHARACTERISTICS

Amplitude
20mV-10V_{pk-pk}, output open circuit
10mV-5V_{pk-pk}, into 50Ω

Resolution
4 digits

Accuracy (at 1kHz)
1V-5V_{pk-pk}: ±(1%+25mV)
100mV-999.9mV_{pk-pk}:±(1%+5mV)
10mV-99.99mV_{pk-pk}:±(1%+2mV)

DC Offset Range
0 to ± 2.495V, 5mV steps

DC Offset Accuracy
±(2%+10mV)

Output Impedance
50Ω±1%

Low-Pass Filter
150MHz, 7-pole, elliptic

Standby (Output Disconnected)
Output On or Off

Output Protection
Short circuit

Glitch Energy
100pV-s at 5V_{pk-pk}

STANDARD WAVEFORMS

(Sine, Triangle, Square, Pulse [Standard, SINC, Exponential and Gaussian], Noise, DC)

Frequency Resolution
7 digits

Accuracy & Stability
Same as frequency standard

Sine

Frequency Range
100µHz to 200MHz, usable to 250MHz

Total Harmonic Distortion (4096 points, 500MS/s)
0.5%

Harmonics (4096 points)

Frequency	Harmonic Level
<200MHz	<25dBc
<10MHz	<40dBc
<100kHz	<50dBc

Band Flatness
<100MHz: 10% (0.83dB)
<200MHz: 30% (2.3dB)

Start Phase Range
0-360°

Square

Frequency Range
100µHz to 200MHz; usable to 250MHz

Duty Cycle Range
1% to 99%

Rise/Fall Time (10%-90%)
<2.5ns

Aberration
<5%

Triangle

Frequency Range
100µHz to 5MHz, usable to 50MHz

Start Phase Range
0-360°

Pulse and Ramp Functions

Frequency Range
100µHz to 5MHz, usable to 50MHz

Delay, Rise/Fall Time, High Time Ranges
0%-99.9% of period (each independently)

Gaussian Pulse Time Constant Range
10-200

Sinc Pulse "Zero Crossings" Range
4-100

Exponential Pulse Time Constant Range
-100 to 100

Noise Function

Frequency Range
100µHz to 5MHz, usable to 50MHz

DC Output Function

Range
-100%-100% of amplitude

ARBITRARY WAVEFORMS

(Waveform memory may be segmented allowing storage of multiple waveforms.)

Custom Waveform Creation Software
WaveCAD software allows instrument control and creation of custom waveforms either freehand, with equations, built-in functions, or imported waveforms.

Feature Placement Resolution
20ps

Waveform Memory
1Meg-points

Vertical Resolution
12 bits (4096 levels)

Number of Memory Segments (Max)
4096

Minimum Segment Size
16 points

SEQUENCED ARBITRARY WAVEFORMS

Operation
Permits division of waveform memory into smaller segments. Segments may be linked and repeated in a user-selectable fashion to generate extremely long waveforms. Sample clock is selectable for each segment. Sample clock changes coherently between steps.

3162B Specifications

Modes

Automatic Sequence Advance

No trigger required to step from one segment to the next. Sequence is repeated continuously per a pre-programmed sequence table.

Stepped Sequence Advance

Current segment is sampled continuously until a trigger advances the sequence to the next programmed segment and sample clock rate.

Single Sequence Advance

First trigger samples the current segment the number of times specified by the repeat (loop) parameter then idles at the value of the last point output. Next trigger advances to the next segment and the process repeats.

Random Sequence Advance

Active segment is controlled in real-time via the front panel D-sub connector. An 8-bit binary word at this connector controls the next segment to advance to.

Jitter Sequence

A portion (such as an edge) of a user-defined waveform is selected and jitter is defined for the specified area. Requires WaveCAD.

Sequencer Steps

1 to 4096

Segment Loops

1 to 1Meg

Segment Duration (min)

100ns, for >1 loop

SAMPLING CLOCK

Internal Source Range

100mHz to 500MHz

Resolution

7 digits

Accuracy and Stability

Same as reference

10MHz Reference Sources

Internal: 1ppm accuracy (19°C-29°C)
1ppm/°C, (<19°C/>29°C)
1ppm/year aging rate
External: Front panel BNC (10MHz, nominal)

SYNTHESIZER AGILITY

Frequency Hopping

Permits the selection of the sampling clock dividing ratio in real time. Sample clock hops (coherently) between up to 256 pre-defined rates.

Hop Control Source

Frequency: Front panel D-sub connector (8-bit binary word)
Trigger: Front panel BNC, TTLTrg0-3 or ECLTrg0

Sampling Clock Range

100mHz to 300MHz: Sampling Clock Division Available
300MHz to 500MHz: Sampling Clock Division Not Available

Ratio Between Carrier and Hop Frequencies

1 to 64k

Hop Table

256 hop frequencies

Hop Delay

Last cycle complete + 150ns

OPERATING MODES

Normal Mode

Continous output of a waveform.

External Triggered Mode

An external signal triggers one output cycle.

Internally Triggered Mode

An internal timer repetitively triggers one output cycle at a fixed interval.

Gated Mode

External signal enables generator output. First gated output cycle is synchronous with the active slope of the triggering signal. Last output cycle is always completed.

Internal Burst Mode

An internal timer repetitively triggers a burst of up to 1Meg output cycles.

External Burst Mode

An external signal triggers a burst of up to 1Meg output cycles.

Delayed Trigger Mode

Trigger takes effect after a pre-defined delay ranging from 1 to 8Meg clock cycles.

TRIGGER CHARACTERISTICS

Input Sources

Internal: 1mHz-50kHz timer
Accuracy: ±(1%+.5µs)
External: Front Panel BNC
VXI Backplane: TTLTrg0-3, ECLTrg0
Software: *TRG

Trigger Programmed Delay

Accuracy: ±(2 clock cycles+system delay)
Resolution: 1 clock cycle
Jitter: 1 clock cycle

Trigger Level Range

Range: ±10V
Resolution: 50mV
Sensitivity: 200mV$_{pk\text{-}pk}$

Input Frequency Range

DC to 18.75MHz

Sync Out

Front Panel: BNC
VXI Backplane: TTLTrg0-3, ECLTrg0

Sync Out Sources

BIT: Selected point in segment.
LCOM: Loop complete.
SSYN: Scope sync. Eliminates ±1 clock jitter.

SYSTEM DELAY

(trigger I/P to waveform O/P)

Trigger Delay Mode OFF

1 sample clock cycle+150ns

Trigger Delay Mode ON

2 sample clock cycle+150ns

PLL CHARACTERISTICS

Operation

Automatically locks output to external signal.

Input Frequency Range

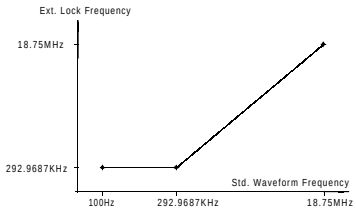
100Hz to 18.75MHz

PLL Input Characteristics

Same as TRIG IN

External Lock Frequency Range

Standard Waveforms: See curve below.



Phase Offset Range

0°-360°

Resolution

2880°/Number of points in waveform

FREQUENCY COUNTER

Operation

Made available to the user in PLL mode only. Frequency reading is valid only when PLL ON LED is lit.

Range

100Hz to 18.75MHz.

Resolution

6 digits

AM CHARACTERISTICS

Input Source

Front Panel BNC

Bandwidth

DC to 1MHz

Modulation Range

0 to 200%

Modulation Sensitivity

0 to -2V generates 100% modulation
0 to -4V generates 200% modulation

3162B Specifications

PM CHARACTERISTICS

Operation

External signal offsets phase. PM input works in PLL mode only.

PM Input

Impedance: 1MΩ, ±5%
Sensitivity: 24°/V, typical
Accuracy: ±10%

FSK CHARACTERISTICS

Operation

Current segment is sampled continuously. External low level (<trigger level) selects sampling clock, external high level (>trigger level) programs shifted frequency. Clock frequency changes coherently.

Carrier Sampling Clock Range

100mHz to 300MHz

FSK Input

Front Panel BNC

Bandwidth

DC to 10MHz

Delay (min)

1 Waveform Cycle

FREQUENCY HOPPING

Operation

Permits the selection of the sampling clock dividing ratio from a hop table with up to 256 entries.

Hop Control Source

Data: Front Panel D-sub
Trigger: Front Panel Trig, TTLTrg0-3, ECLTrg0

Sample Clock Selection

Data: Binary combination of 8 data lines determines frequency divider.
Trigger: Trigger advances to the next of the hop table.

Carrier Sampling Clock Range

100mHz to 300MHz

Hop Table

256 Hop Frequencies

Hop Delay

Last Waveform Complete + 100ns

FRONT PANEL I/O

Main Output (1 and 2)

Connector/Z_{out}: BNC/ 50Ω ±1%
Protection: Short Circuit to Case

Sync Output

Connector/Z_{out}: BNC/50Ω ± 1%
Level: >2V into 50Ω, 5V into 10kΩ
Protection: Short Circuit to Case

Trigger/FSK/PLL Input

Connector/Z_{in}: BNC/10kΩ ±5%
Slope: Positive or Negative (selectable)
Input Voltage: ±12V
Pulse Width (min.): 20ns

AM/PM Inputs (1 and 2)

Connector/Z_{in}: BNC/1MΩ ±5%
Protection: ±12V
AM Input Range: 0 to -4V
PM Input Range: 24°/V, typical

External Reference Input

Connector/Z_{in}: BNC/10kΩ ±5%
Threshold Level: TTL
Pulse Width (Min.): 20ns

Frequency/Segment Hop Data Input

Connector: 9-pin D-sub, Male
Threshold Level: TTL

VXIbus INTERFACE DATA

(Single-slot, Message-based, VXIbus 1.4 Compliant)

Software Compliance

SCPI 1993.0, IEEE488.2

Drivers

LabVIEW, LabWindows/CVI, VXI*plug&play* (WIN, WIN95, WIN NT Frameworks)

Waveform Creation & Control Software

WaveCAD (WIN, WIN95, WIN NT)

Shared Waveform Memory

A32 VME block transfer

Backplane Signal Support

TTLTrg0-3: Trigger In, Sync Out
ECLTrg0: Trigger In, Sync Out

Status Lights

Red: Power-On Self-Test Failure
Green: Module accessed on VXIbus
Yellow: Phase Lock is engaged
Green: Output on

Cooling (10°C Rise)

4.9 l/s@0.14mm H_20

Peak Current & Power Consumption

	+24	+12	+5	-2	-5.2	-12	-24
I_{Pm}(A)	0.15	1.0	6.0	2.0	11	1.0	0.15
I_{Dm}(A)	0.025	0.25	1.0	0.25	2.0	0.25	0.025

Total Power: 123 Watts

ENVIRONMENTAL

Temperature

Operating: 0°C-50°C
Storage: -40°C-70°C
Spec Compliance: 20°C-30°C, 30min. warm-up

Humidity (non-condensing)

11°C-30°C: 95% ±5%
31°C-40°C: 75% ±5%
41°C-50°C: 45% ±5%

Altitude

Operating: 10,000ft.
Storage: 15,000ft.

Vibration (non-operating)

2g at 55Hz

Shock (non-operating)

30g, 11ms, half sine pulse

Weight

3162A: 3lbs. 8oz. (1.6kg)
3162B: 4lbs 8 oz. (2.2kg)

EMC (Council Directive 89/336/EEC)

EN55011, Group1, Class A, EN50082-1, IEC 801-2,3,4

Safety (Low Voltage Directive 73/23/EEC)

EN61010-1, IEC1010-1, UL3111-1, CSA 22.2#1010

ORDERING INFORMATION

Model	Description	Part Number
3162B	500 MS/s Freq. Agile Waveform Sythesizer, 1MEG	407629-012
3162B, 4MEG	500 MS/s Freq. Agile Waveform Sythesizer, 4MEG	407629-013
3162B, 8MEG	500 MS/s Freq. Agile Waveform Sythesizer, 8MEG	407629-014

CE The CE Mark indicates that the product has completed and passed rigorous testing in the area of RF Emissions, Immunity to Electromagnetic Disturbances and complies with European electrical safety standards.

The Racal policy is one of continuous development and consequently the equipment may vary in detail from the description and specification in this publication.

RACAL INSTRUMENTS

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